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| EXAMINER |
|---|
| NGUYEN, HIEP |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/606,367 | CHEN ET AL. | |
| | Examiner | Art Unit | |
| | Hiep Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-7 and 10-25* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 6/28/00 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitations " a sense amp" in claim 3, " a pull-down terminal", "a pull-up terminal", " a first inverter" "a second inverter" a third inverter", "a fourth inverter" in claim 5, " a differential domino circuit" in claim 10, " a plurality of data paths" in claim 17, " said processor comprises a processor" in claim 21, "a microprocessor" in claim 22, " a network processor" in claim 23, " a digital signal processor" in claim 24 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

Claim 8 is objected to because of the following informalities: the recitation " said output terminals" on line 4 does not have antecedent basis. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10 and 19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Figure 6 of the present application shows a static or domino full swing logic circuit

(630) coupled to the differential sense latch (620). Assume that the static or domino full swing logic circuit (630) is the "differential domino circuit" shown in figure 3 (prior art) then it is impossible to incorporate this "differential domino circuit" to the differential sense latch (620) in figure 6 or to the circuits of figure 4 or 5 because the input/output pins are not compatible. For example, figure 3 shows a full-swing logic (630) having 6 input pins. Figure 6 shows only two output pins going to the full-swing logic circuit (630).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-10 and 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 3, the recitation "a sense amp" is indefinite because it is unclear as to this "a sense amp" is the same or different than the " a differential sense circuit" in claim 1. If it is different, it is unclear as to how the combination of claims 1 and 3 would read on any preferred embodiment of the invention. Applicant is required to particularly point out the figure that read on both claim 1 and 3 combined.

Regarding claim 5, the connections of the components are confusing for instance lines 3-4 shows that the input terminals of the first and second inverters are coupled to **a pull-down terminal** (not shown in the drawing). Lines 6-8 show that the input terminals of the first and second inverters are coupled to **a non-inverted output terminal and an inverted output terminal** of the p-type sense amplifier. Lines 4-5 recites that the output terminals of the first and second inverters are coupled to **a pull-up terminal**. Lines 5-6 recites that the output terminals of the first and second inverters are coupled to **opposite terminals of the said latch.** According to the language of the claim, it appears that the " a pull-down terminal" is connected to the "a non-inverted output terminal and an inverted output terminal of the p-type sense amplifier" and the "a pull-up terminal" is connected to the "opposite terminals of the said latch". The third and fourth inverters are not shown in the drawing. Note that in figure 5, (540, 580) and (560, 570) are not inverters because the connections are not configured to make theses transistors be inverters. The

Applicant is requested to point out which drawing the circuit of claim 5 reads on. The applicant is also requested to point out in the corresponding drawing the first, second, third and fourth transistors, the pull-up terminal, the pull-down terminal. Quoting from the detailed description, page 10, lines 27-29, does not make any sense thus, it cannot solve the 112, 2nd problem of claim 5.

Regarding claim 6, the recitation "said inverters" is indefinite because it is unclear "said inverters " comprises which inverters. Figure 4 of the present application shows only two inverters (405, 410, 415) and (420, 425, 430) besides the two inverters of the latch (480). Figure 5 of the present application shows only inverters (520, 530) besides the two inverters of the latch (590). Thus, there are no four inverters besides the inverter of the latches as recited in claims 5 and 6.

Regarding claim 10, the recitation "further comprising a differential domino circuit...to be stored in said differential sense latch" is indefinite because it is not clear what is the "a differential domino circuit". Figures 4 and 5 of the present application show only sense amplifier and inverters. There is no differential domino circuit coupled to the differential sense latch to perform the recited function. The applicant is requested to point out in the circuit the "a differential domino circuit", the "differential output terminals" in the drawings. It is unclear whether the "differential output signals" are the differential output signals of the "a circuit" or the "differential latch circuit" or the "a latch".

Regarding claim 21, the recitation "wherein said processor comprises a network processor" is indefinite because it is misdescriptive. None of the drawings of the present application shows an IC circuit **comprising** a processor. Figure 6 of the present application shows a processor comprising "an IC circuit".

Claims 4-9 and 22-24 are indefinite because of the technical deficiencies of claims 3 and 21.

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Shieh (US Pat. 5,903,171).

Regarding claim 1, figure 2 of Shieh shows a circuit comprising: a differential sense circuit (100, 105); a latch (145, 150), said latch comprising cross coupled inverters; said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle. Note that the differential sense circuit (100, 105) receive two weak signals (DL) and DL/) and amplifies them to provide stronger signals (col. 3, lines 27-44). Signal (SRE) controls the latch operation. The signals are stored in the latch for at least one clock cycle (col. 3, lines 27-44).

Regarding claims 3 and 7, said sense amp (100, 105) and said differential sense latch (145, 150) coupled such that, in operation, differential signals present on differential output terminals of said sense amp cause an electronic signal to be stored in said differential sense latch (col. 3, lines 27-44). The sense amplifier comprises transistors (100) and (105) that are n-type transistors.

Claims 1, 3-6 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Chung et al. (US Pat. 6,160,742).

Regarding claim 1, figures 3a and 4b of Chung shows a circuit comprising: a differential sense circuit (32, 34); a latch (36), said latch comprising cross coupled inverters (15, 16); said differential sense circuit and said latch being coupled so as to form a differential sense latch (32, 34, 36) such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle. Note that the circuit functions according to a system clock. Based on the clock cycles, data is transferred or processed. Thus, the electronic signal stored in said latch is retained for at least one clock cycle. Moreover, figure 4b of Chung shows that the output data DB/DBB of the latch (13, 14) varies at every cycle of clock (XCK).

Regarding claim 3, figure 3a shows a sense amp (30), said sense amp and said *differential sense latch* (32, 34, 36) coupled such that, in operation, differential signals present on differential output terminals of said sense amp cause an electronic signal to be stored in said differential sense latch.

Regarding claim 4, the sense amp comprises a p-type sense amp (P2, P3).

Regarding claim 5, insofar as understood, figure 3a of Chung show a differential sense circuit comprises: a first inverter (I1) and a second inverter (I2), said first and second inverters each having an input terminal and an output terminal, said input terminal of said first and second inverter being coupled respectively to "a pull-down terminal", said output terminal of said first and second inverters being coupled respectively to "a pull-up terminal", said output terminal of said first and second inverter being respectively coupled to opposite terminals of said latch (36), said input terminal of said first and second inverter being respectively coupled to a non-inverted output terminal and an inverted output terminal of said p-type sense amp (30). The third inverter is (P4, N5) and the fourth inverter is (P6, N6).

Regarding claim 6, circuit (32) has symmetrical configuration thus, the equivalent loads are applied to the outputs of (30).

Regarding claim 25,the differential sense circuit (32, 34) is coupled to latch (36) in a push-pull configuration.

Claims 11-16 are rejected under 35 U.S.C.102 (e) as being anticipated by Takahashi (US Pat. 6037,824).

Regarding claims 11 and 12, figure 7 of Katahashi (6,037,824) shows a method for storing electronic signals produced by a differential circuit comprising: pre-charging said differential circuit (elements N12, N13); evaluating said differential circuit (231); sensing differential output signals via a differential sense circuit (231), wherein said differential sense circuit is coupled to a latch (NA2, NA3) in a push-pull configuration (via 231); and storing an electronic signal corresponding to said differential output signal. Transistors (N34, N35) when activated will pull the output approximately the same voltage (ground level).

Regarding claim 13-16, figure 7 of Takahashi (824) shows a method for storing electronic signals produced by a differential circuit comprising: applying clock (iclkb0) after pre-charging to bring the differential output terminal (the drain of N31 to a power supply voltage Vdd) and applying clock (iclkb3) to bring the differential output terminal (the source of N32 to a ground voltage).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 17, 18 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US Pat. 6,160,742).

Regarding claim 7, figures 3b and 4b of Chung include all the limitations of the present application except for the limitation that the sense amp comprises an n-type sense amp. However, it is old and well known to those having skills in the art that an n-type transistor and a p-type transistor are exchangeable depending on the polarities of the control signals applied to the gates of these transistors or depending on the type of power supplies used. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to change the p-type transistors of the p-type sense amplifier (30) of Chung with the n-type transistors in order to conform to the control signals applied to these transistors.

Regarding claims 17 and 18, figures 3b and 4b of Chung shows a data path comprising a differential circuit (30) generating signals (DA) and (DAB) and a differential sense latch (32, 34, 36), wherein said differential sense latch comprises a differential sense circuit (32, 34) and a jam-latch (36) coupled such that, in operation, an electronic signal based, at least in part, on differential output terminals (N3, N4) of said differential circuit is stored in said jam-latch. Not disclosed is a plurality of data paths. **However, the plurality of cited elements is mere duplication of parts that is not patently distinct. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).** Therefore, it would have been obvious to those skilled in the art to implement a plurality of input circuits for having the capability of handling a plurality of inputs. The sense amp in claim 18 comprises (P2, P3).

Regarding claim 20, latch (36) comprises cross-coupled inverters.

Regarding claim 21-24, the limitations "a processor", "a microprocessor", "a network processor and "a digital processor" are merely intended uses. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQF.2d 1647 (1987). Therefore, this limitation has not been given patentable weight.

***Allowable Subject Matter***

Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8 and 9 are objected to because the prior art of record fails to teach or fairly suggest a differential sense circuit comprising first and second inverters wherein, the clock terminals of the first and second inverters are coupled to respective top n-device of the stacked n-devices in the first and second inverters as called for in claim 8.

***Response to arguments***

In the Remarks, page 8, the Applicant argues that "the elements of Takahashi patent cited by the examiner fails to make a prima facie case of obviousness under the patent status". In fact, the three basic criteria have been met: a) the n-type transistor and the n-type transistor are well known in the art to one of ordinary skill to be exchangeable; b) the n-type or p-type transistors is selected in a circuit because of the characteristics of the control signals (positive or negative); c) the motivation to change the type of transistor or the type of sense amplifier is to conform with the polarities of the control signal applied to the transistor of the sense amplifier. In this case, for the design purpose, if the one of ordinary skill in the art has to use inverting buffers between the circuit of the present application and the other circuit that provides the control signals, he/she will be motivated to switch the p-type sense amplifier to an n-type amplifier in order to conform with the reversing of the polarities of the control signals created by the inverting buffers. Thus, switching from p-type device to n-type device

is merely a design choice, not a novelty. The prima facie case of obviousness under the patent status has been properly established.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
06-04-03

TUAN T. LAM
PRIMARY EXAMINER